IN THE CLAIMS

Claim 1 (currently amended): A multichip module comprising:

a first chip having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire;

a second chip having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire;

a first attach layer having an area equal to an area of said second chip bottom surface for coupling said first chip and said second chip, said first attach layer covering said each of said bonding pads on said first chip and having a thickness to provide electrical disconnection of said first chip wire bonds and said second chip, said first attach layer is applied to said second chip bottom surface prior to coupling said first chip and said second chip; and

a second attach layer having an area equal to said second chip bottom surface area formed without spacers and disposed between said first attach layer and said second chip bottom surface, said second attach layer being an insulating material having a thickness and cooperable with said first attach layer to provide electrical disconnection of said first chip wire bonds and said second chip.

Claim 2 (original): The multichip module of Claim 1, wherein said electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately 10 μm.

Claim 3 (original): The multichip module of Claim 1, wherein said first attach layer is a thermosetting material, wherein said thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond.

Claim 4 (original): Th multichip module of Claim 1, wherein said first chip top and bottom surfaces and said second chip top and bottom surfaces have equal areas.

Claim 5 (original): The multichip module of Claim 1, wherein said first chip and said second chip have a stacked arrangement such that said first chip bonding pads are covered from above by said second chip.

Claim 6 (cancelled)

Claim 7 (previously presented): The multichip module of Claim 1, wherein said first attach layer is a thermosetting material, wherein said thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond and said second attach layer is silicon dioxide.

Claim 8 (previously presented): The multichip module of Claim 1, wherein said electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately equal to said second attach layer thickness.

Claim 9 (previously presented): The multichip module of Claim 1, wherein said second attach layer thickness is approximately 1 μm.

Claim 10 (previously presented): The multichip module of Claim 6, wherein said first chip top and bottom surfaces and said second chip top and bottom surfaces have equal areas, and wherein said first and second chips are stacked such that said first chip bonding pads are covered from above by said second chip.

Claim 21 (currently amended): A multichip module, comprising:

a first chip having opposing top and bottom surfaces and having first bonding pads located on a perimeter of said top surface;

a wire having a bond to one of said first bonding pads;

a second chip having opposing top and bottom surfaces and positioned with said bottom surface of said second chip adjacent said top surface of said first chip;

a first attach layer between said top surface of said first chip and said bottom surface of said second chip and covering said wire bond, said first attach layer having an area substantially equal to the area of said second chip formed without spacers; and

a second attach layer adjacent to said bottom surface of said second chip and between said bottom surface of said second chip and said first attach layer.

Claim 22 (cancelled)

Claim 23 (previously added): The multichip module of Claim 21, wherein said first attach layer is a thermosetting material.

Claim 24 (previously added): The multichip module of Claim 21, wherein said second attach layer is an inorganic material.

Claim 25 (previously added): The multichip module of Claim 21, wherein said first and second chips are approximately the same size.

Claim 26 (previously added): A multichip module, comprising:

a substrate having a plurality of contact pads;

a first chip having opposing top and bottom surfaces and having first bonding pads located on a perimeter of said top surface, said first chip mounted on said substrate;

a wire having a ball bond to one of said plurality of contact pads on said substrate and a bond to one of said first bonding pads;

a second chip having opposing top and bottom surfaces and positioned with said bottom surface of said second chip adjacent said top surface of said first chip;

a first attach layer between said top surface of said first chip and said bottom surface of said second chip and covering said wire bond to said one of said first bonding

pads, said first attach layer having an area substantially equal to the area of said second chip;

a second attach layer adjacent to said bottom surface of said second chip and between said bottom surface of said second chip and said first attach layer.

Claim 27 (cancelled)

Claim 28 (previously added): The multichip module of Claim 26, wherein said first attach layer is a thermosetting material.

Claim 29 (previously added): The multichip module of Claim 26, wherein said second attach layer is an inorganic material.

Claim 30 (previously added): The multichip module of Claim 26, wherein said first and second chips are approximately the same size.